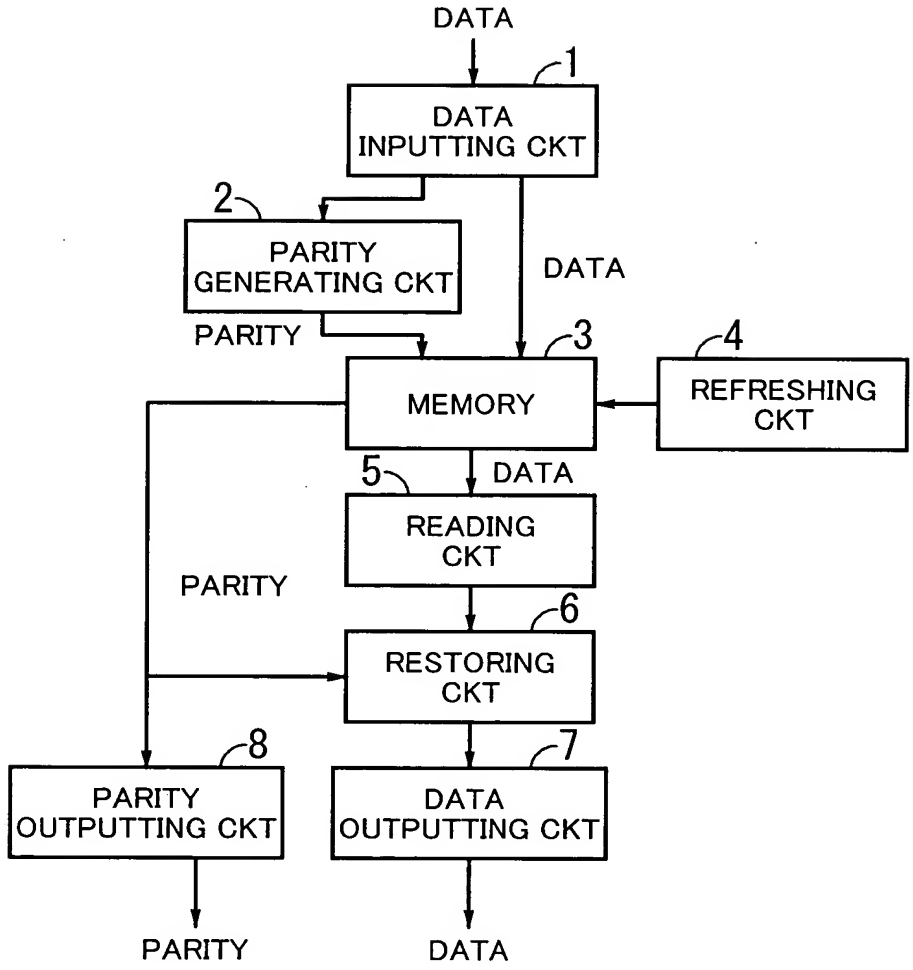

FIG. 1

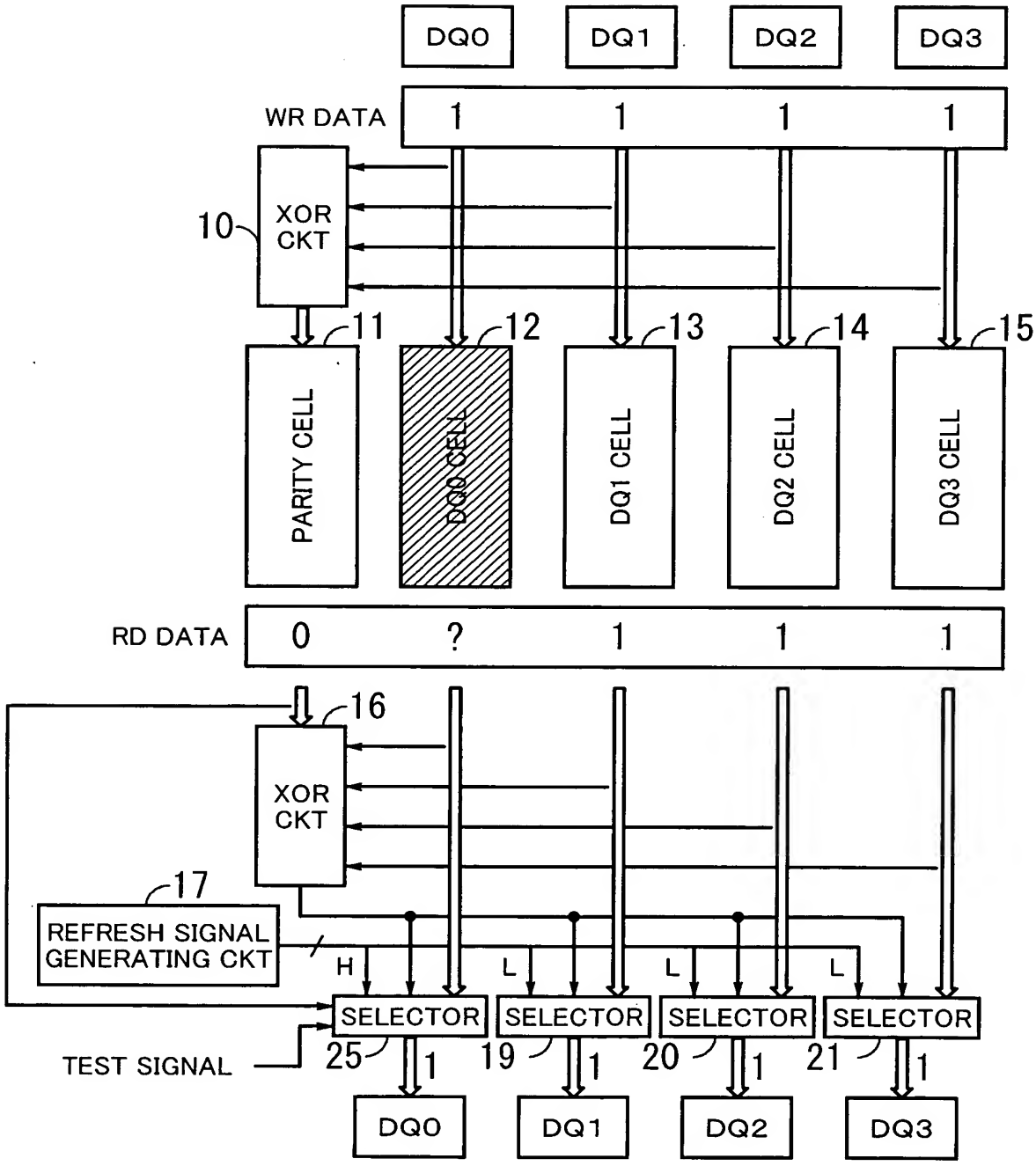
DQ0
DQ1
DQ2
DQ3
WR DATA
1
1
1
1
10
XOR CKT
11
12
13
14
15
PARITY CELL
DQ0 CELL
DQ1 CELL
DQ2 CELL
DQ3 CELL
RD DATA
0
?
1
1
1
16
XOR CKT
17
REFRESH SIGNAL GENERATING CKT
H
L
L
L
SELECTOR
SELECTOR
SELECTOR
SELECTOR
TEST SIGNAL
25
19
20
21
1
1
1
1
DQ0
DQ1
DQ2
DQ3

FIG. 2

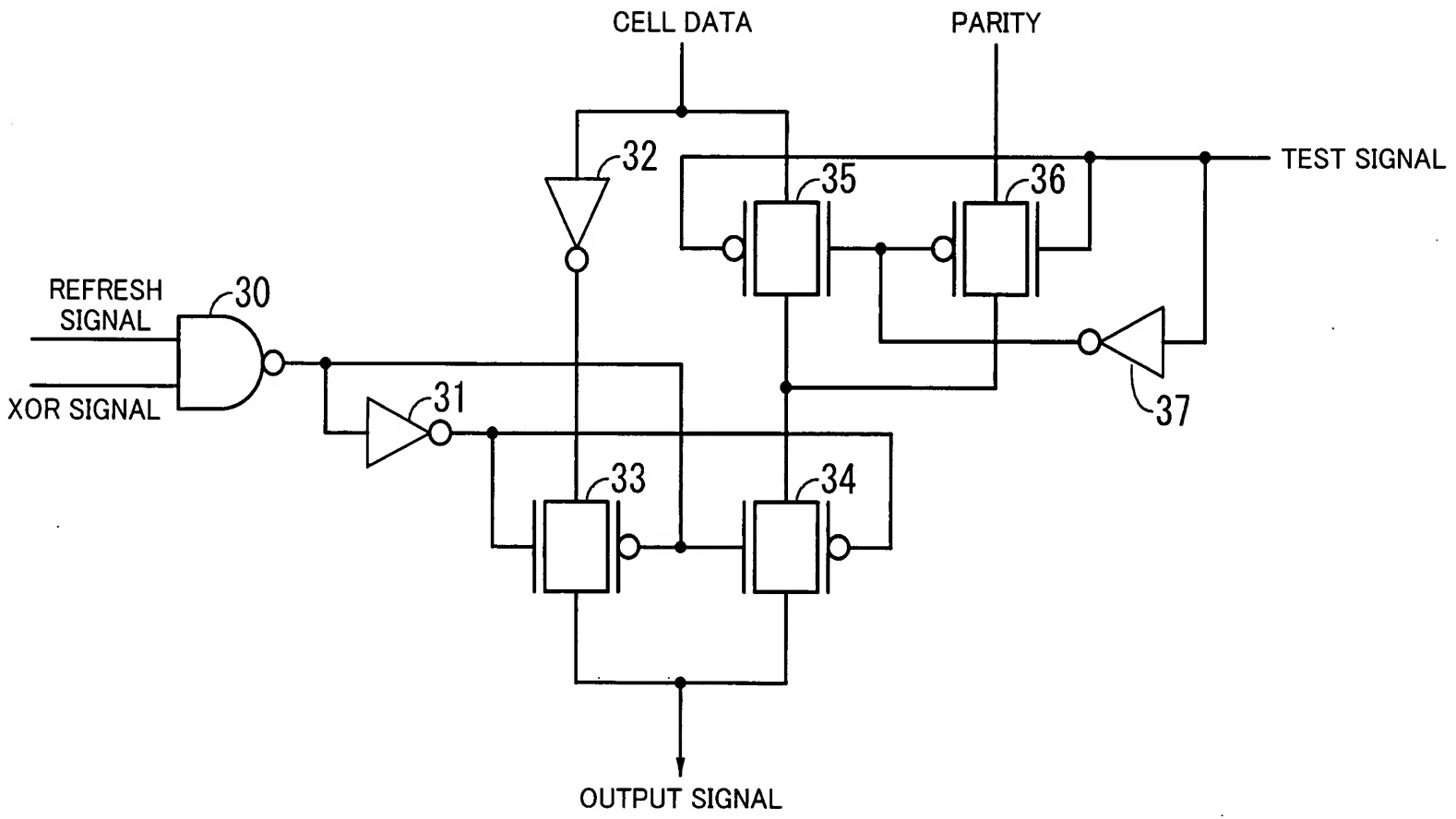

FIG. 3

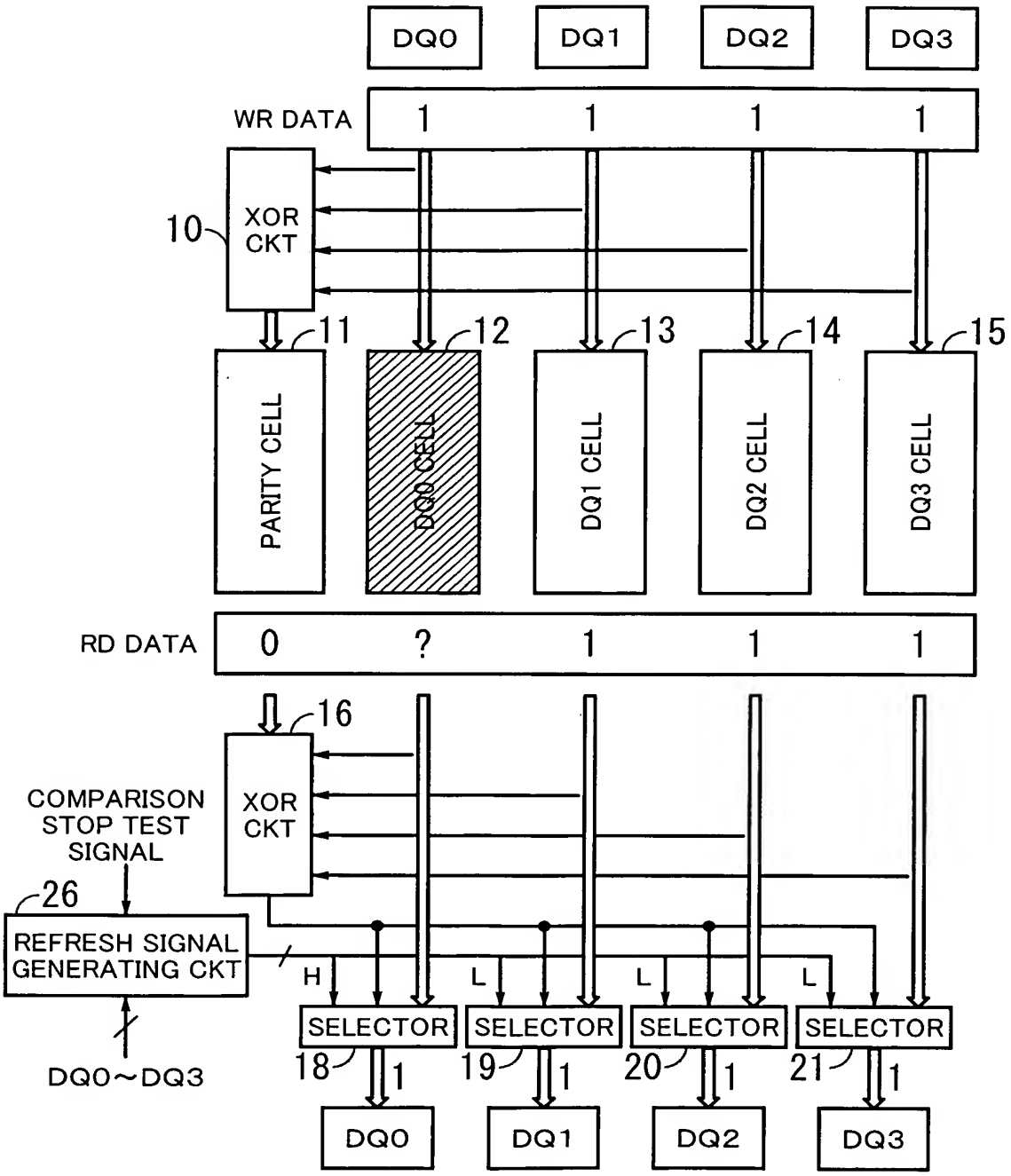
DQ0
DQ1
DQ2
DQ3
WR DATA
1
1
1
1
10
XOR CKT
11
12
13
14
15
PARITY CELL
DQ0 CELL
DQ1 CELL
DQ2 CELL
DQ3 CELL
RD DATA
0
?
1
1
1
16
XOR CKT
COMPARISON STOP TEST SIGNAL
26
REFRESH SIGNAL GENERATING CKT
DQ0~DQ3
H
L
L
L
SELECTOR
SELECTOR
SELECTOR
SELECTOR
18
19
20
21
1
1
1
1
DQ0
DQ1
DQ2
DQ3

FIG. 4

PARITY CHECK TEST SIGNAL DQ0
PARITY CHECK TEST SIGNAL DQ1
PARITY CHECK TEST SIGNAL DQ2
PARITY CHECK TEST SIGNAL DQ3
COMPARISON STOP TEST SIGNAL
INTERNAL REFRESH ADDRESS SIGNAL DQ0
INTERNAL REFRESH ADDRESS SIGNAL DQ1
INTERNAL REFRESH ADDRESS SIGNAL DQ2
INTERNAL REFRESH ADDRESS SIGNAL DQ3
REFRESH SIGNAL DQ0
REFRESH SIGNAL DQ1
REFRESH SIGNAL DQ2
REFRESH SIGNAL DQ3
50
51
52
53
54
55
56
57
58
59
60
61
62

FIG. 5

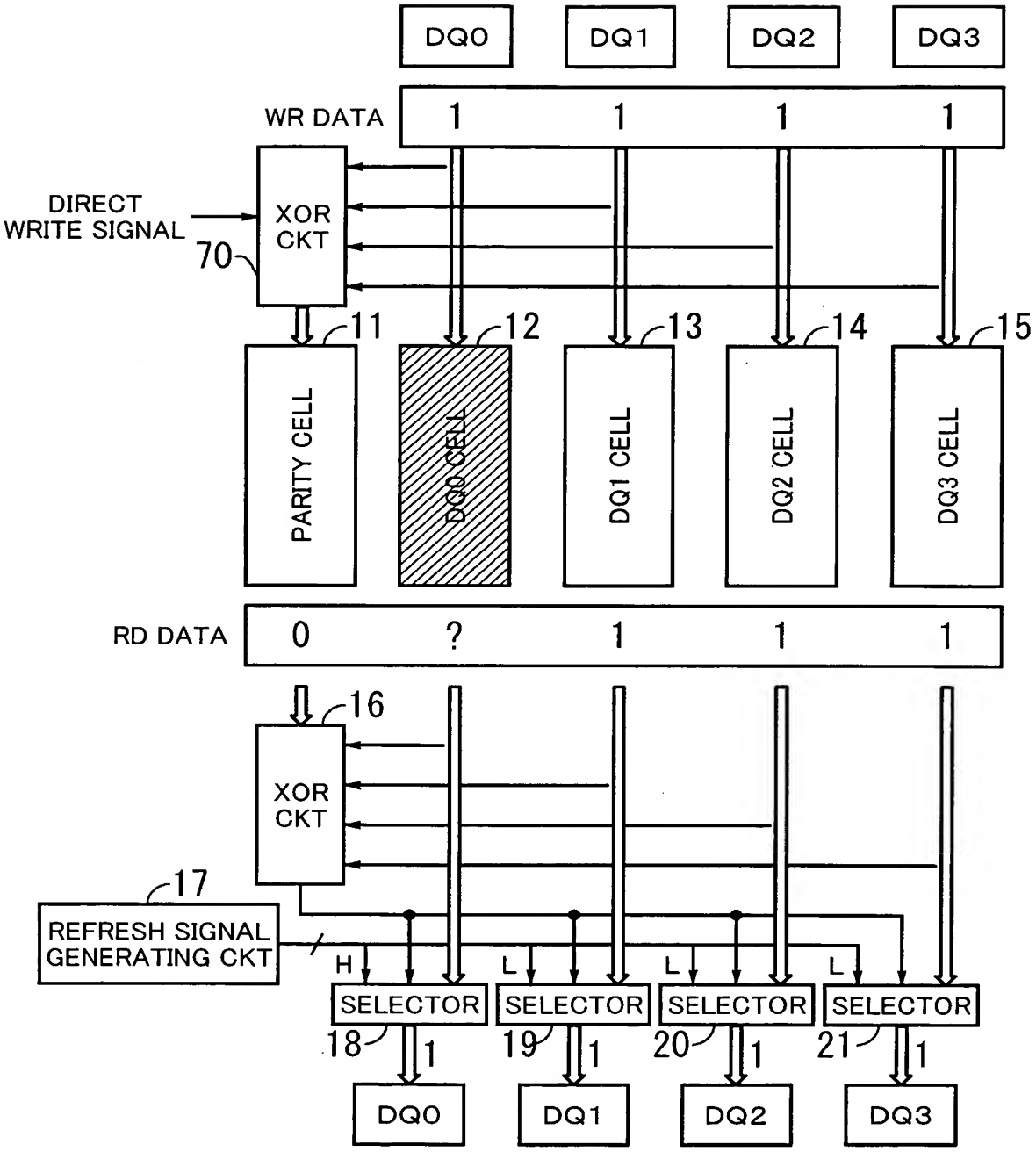

FIG. 6

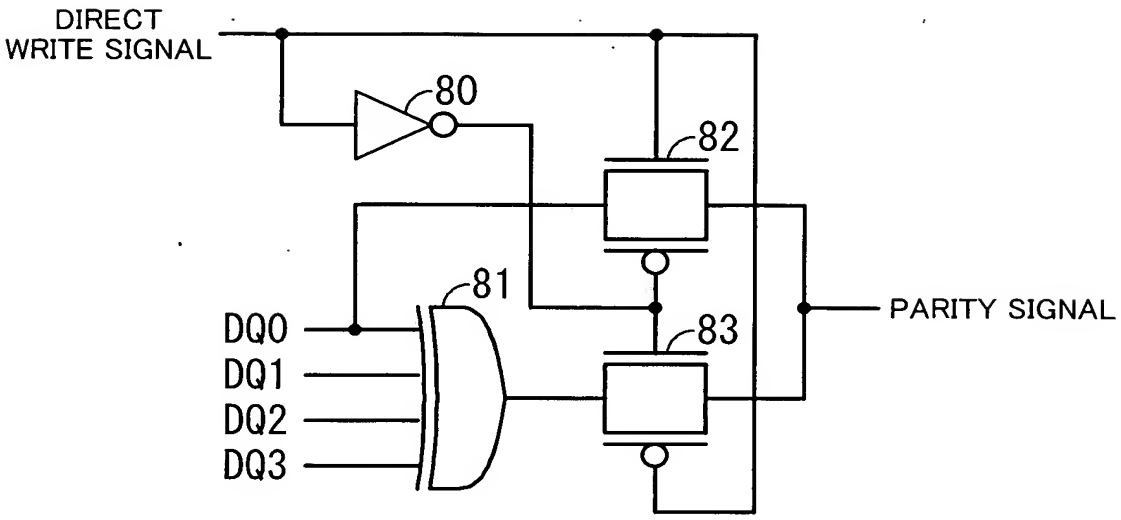

FIG. 7

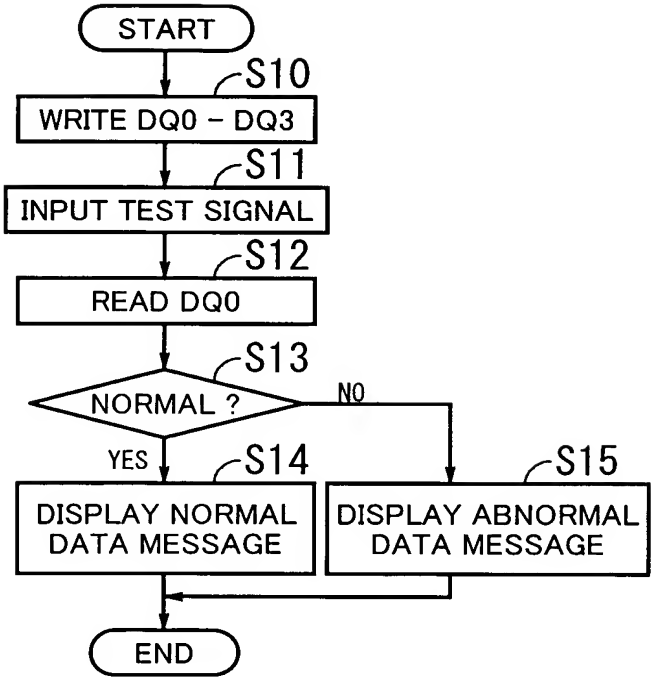

FIG. 8

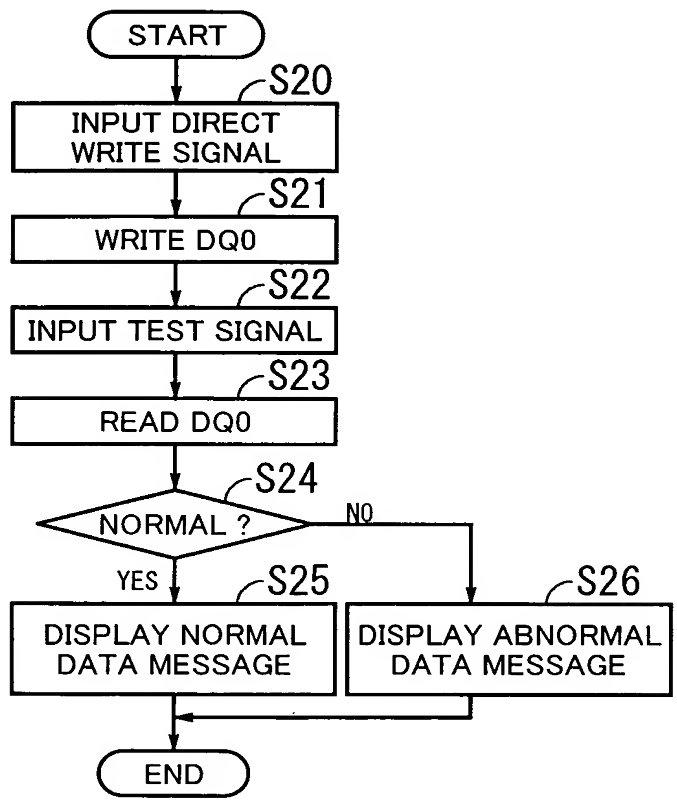

FIG. 9

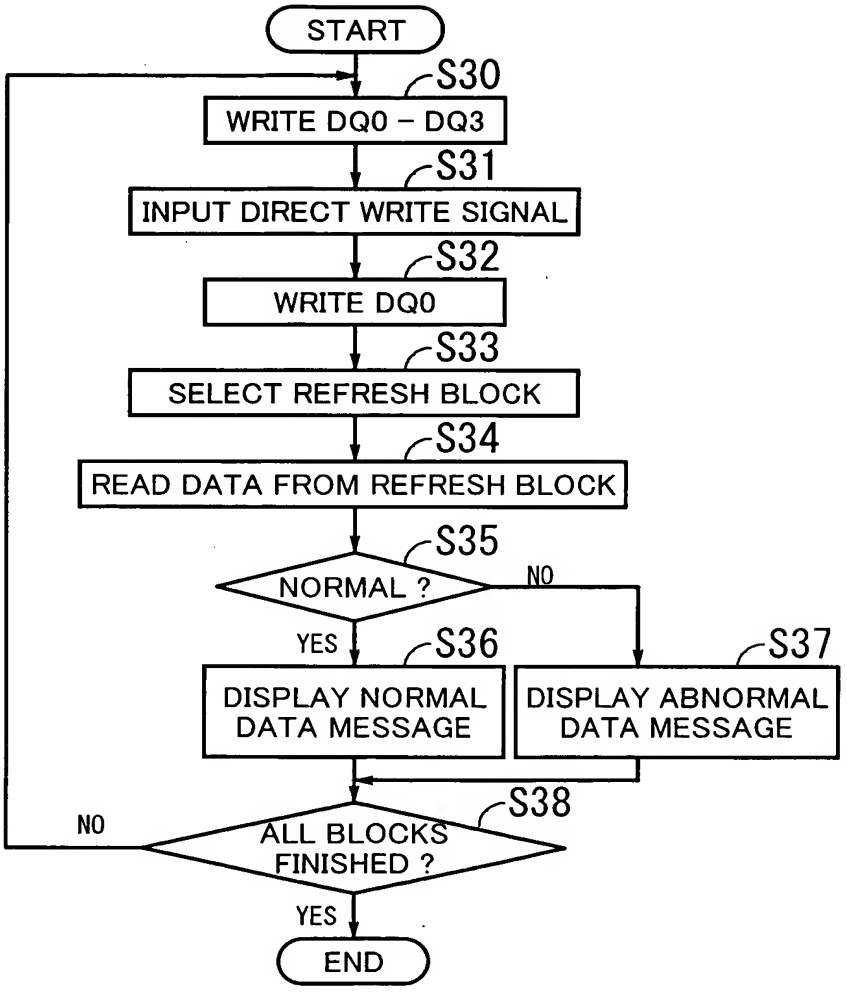

FIG. 10

MEMORY ARRAY				PARITY ARRAY
1−1	1−2	1−3	1−4	1P
2−1	2−2	2−3	2−4	2P
3−1	3−2	3−3	3−4	3P
4−1	4−2	4−3	4−4	4P

FIG. 11

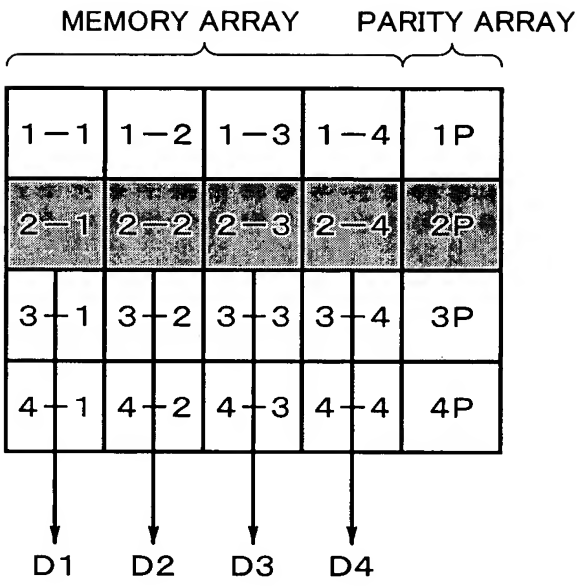

FIG. 12

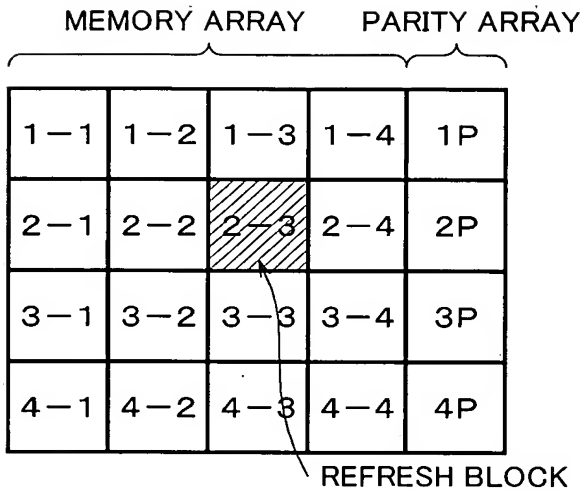

FIG. 13

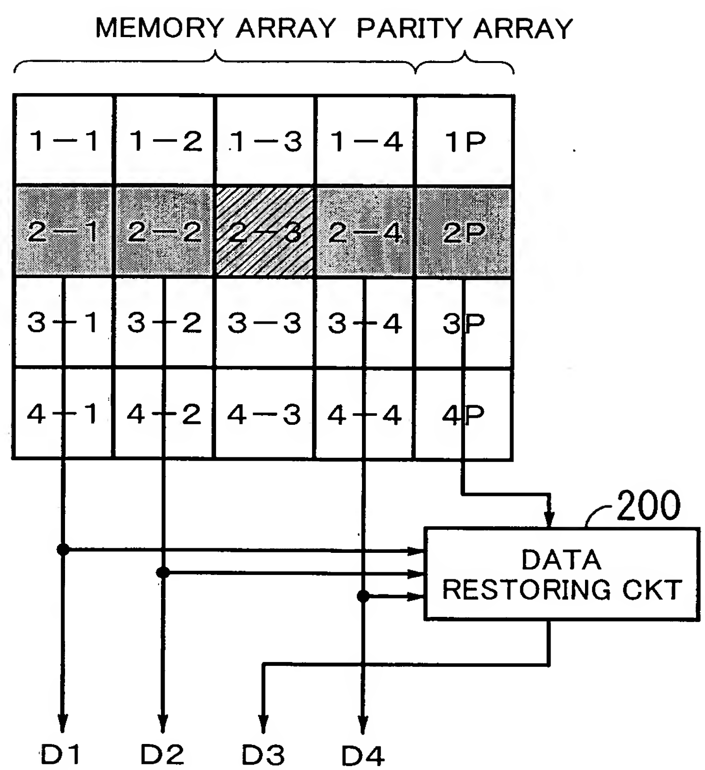

FIG. 14

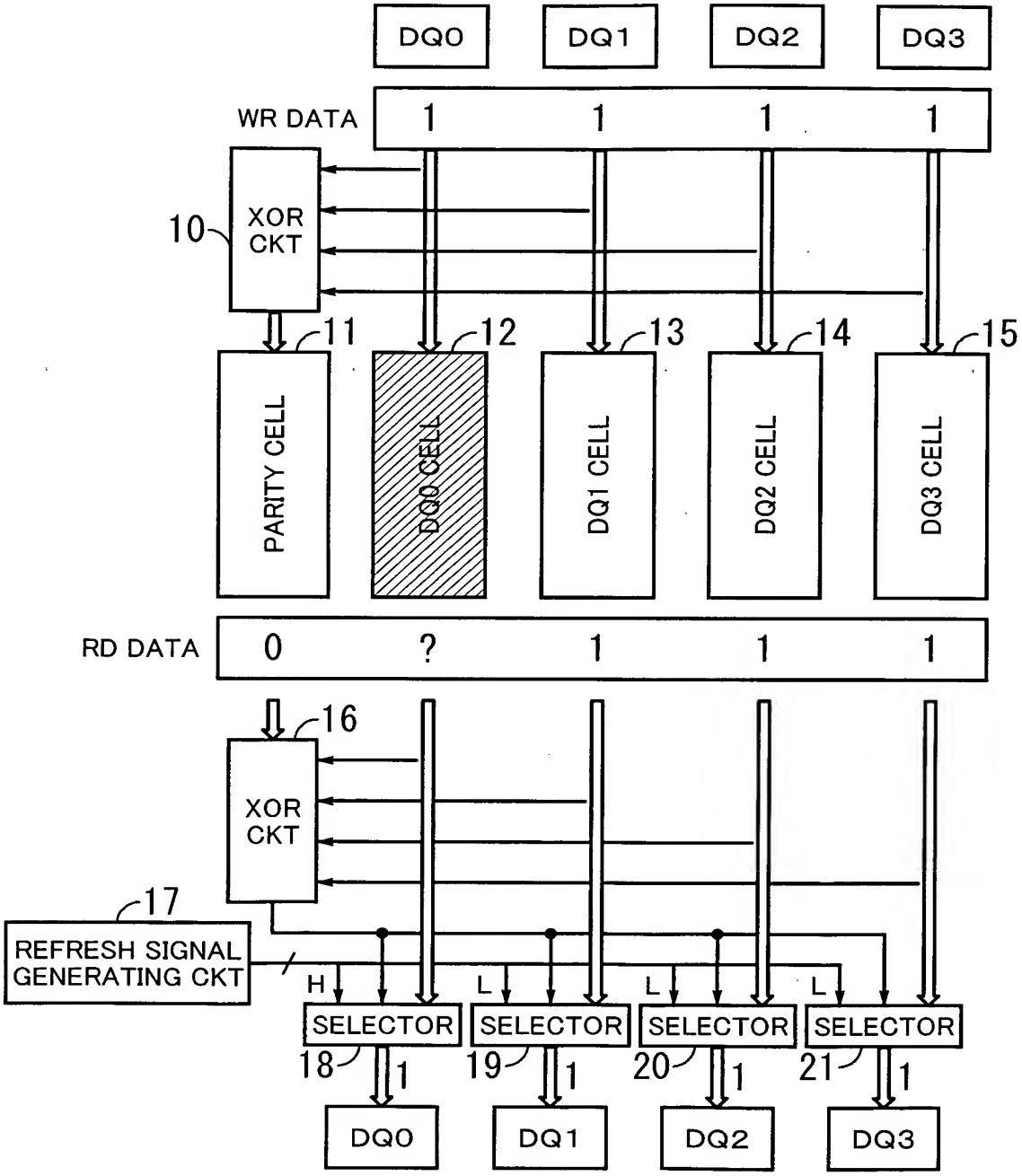
DQ0
DQ1
DQ2
DQ3
WR DATA
1
1
1
1
10
XOR CKT
11
12
13
14
15
PARITY CELL
DQ0 CELL
DQ1 CELL
DQ2 CELL
DQ3 CELL
RD DATA
0
?
1
1
1
16
XOR CKT
17
REFRESH SIGNAL GENERATING CKT
H
L
L
L
SELECTOR
SELECTOR
SELECTOR
SELECTOR
18
19
20
21
1
1
1
1
DQ0
DQ1
DQ2
DQ3

FIG. 15

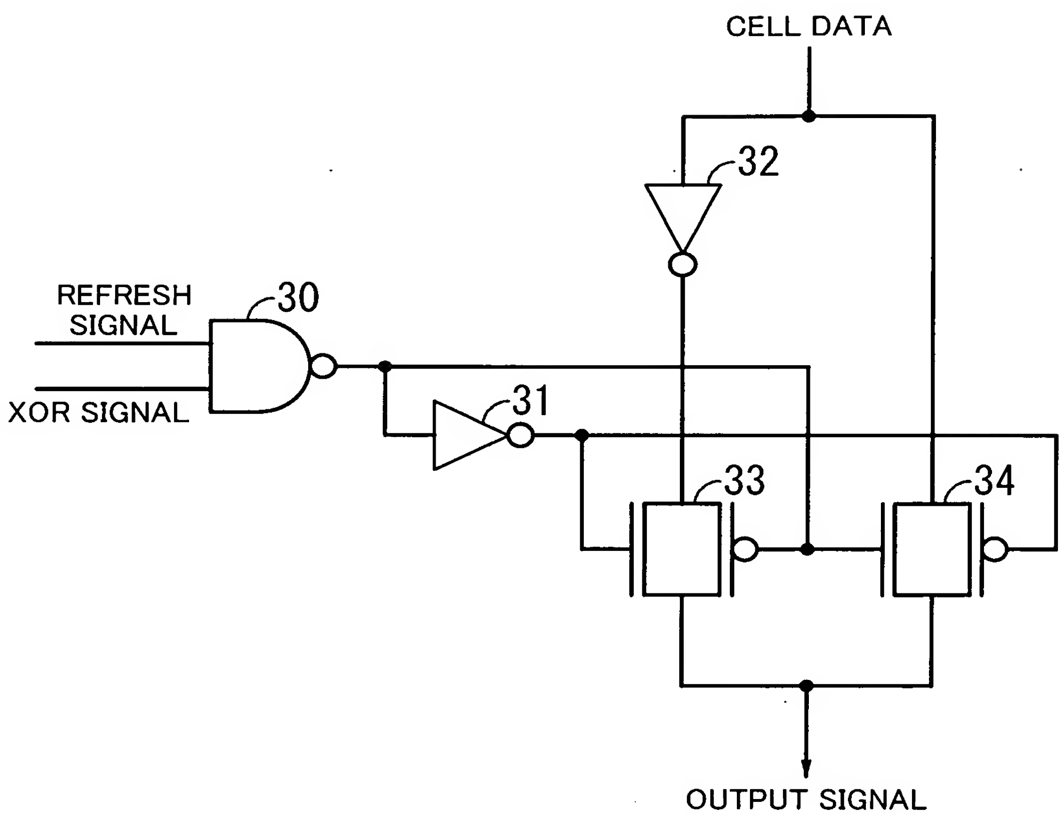

FIG. 16